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20872 7590 05/09/2006

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Sheena Hicks (Depositor's name)
Sheena Hicks (Signature)
 June 23, 2006 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,085	09/29/2003	Elinas Fallon	188122003600	2168

TITLE OF INVENTION: METHOD FOR GENERATING CONSTRAINED COMPONENT PLACEMENT FOR INTEGRATED CIRCUITS AND PACKAGES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES NO	\$700 \$1,400	\$300	\$1000 \$1,700	08/09/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
ROSSOSHEK, YELENA	2825	716-010000 01 FC:1501

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cadence Design Systems, Inc.

San Jose, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
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- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☒ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature

Date June 23, 2006

Typed or printed name Thomas Chan

Registration No. 51,543

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FROM: Thomas Chan

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Number of pages with cover page:	3	
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Preparer of this slip has confirmed that facsimile number given is correct: 12135/srh2

Comments:

OFFICIAL FILING

Attorney Docket No.: 188122003600
Group Art Unit: 2825
Examiner: Y. Rossoshek
Serial No.: 10/674,085
Filing Date: September 29, 2003
Inventor: Elias FALLON et al.
Title: METHOD FOR GENERATING CONSTRAINED
COMPONENT PLACEMENT FOR INTEGRATED
CIRCUITS AND PACKAGES

Papers enclosed herewith:

1. Part B - Fee(s) Transmittal + duplicate copy for fee processing - 2 pages

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